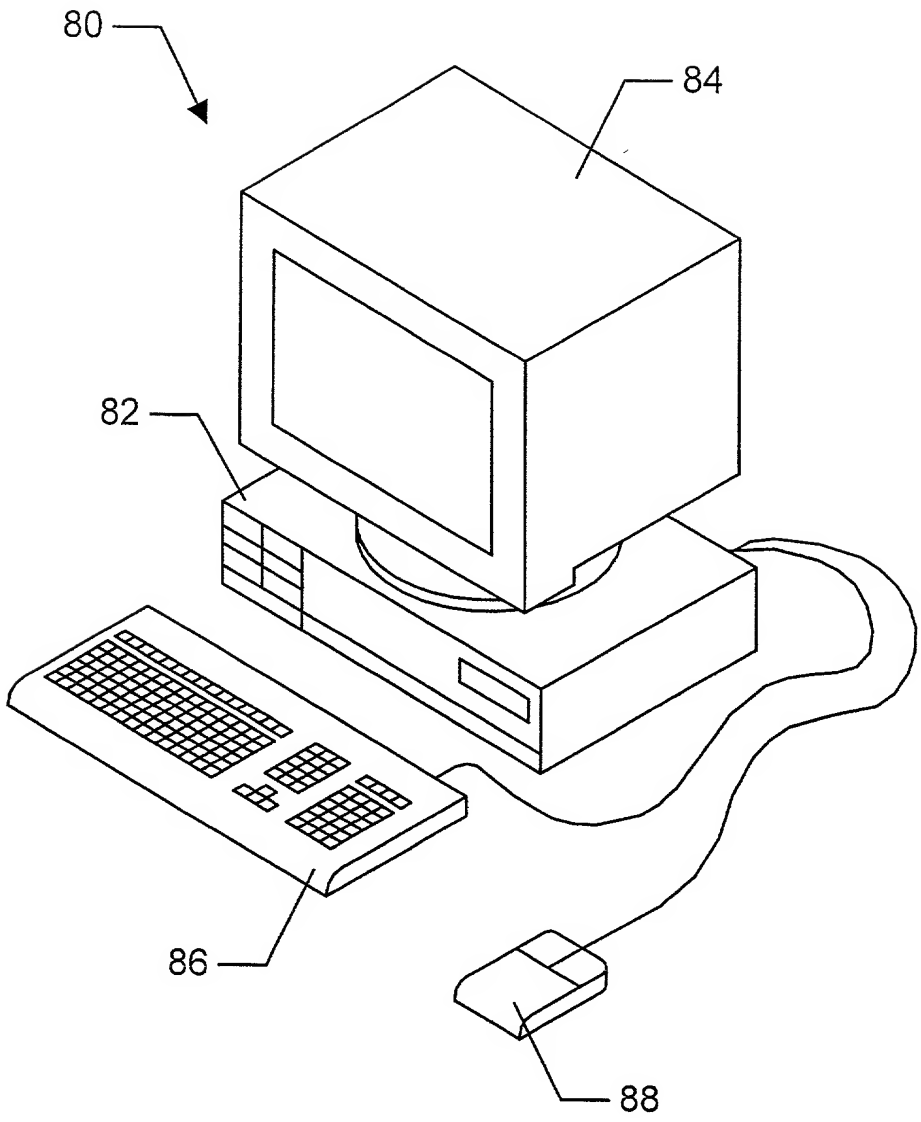

FIG. 1

208220 9E95801

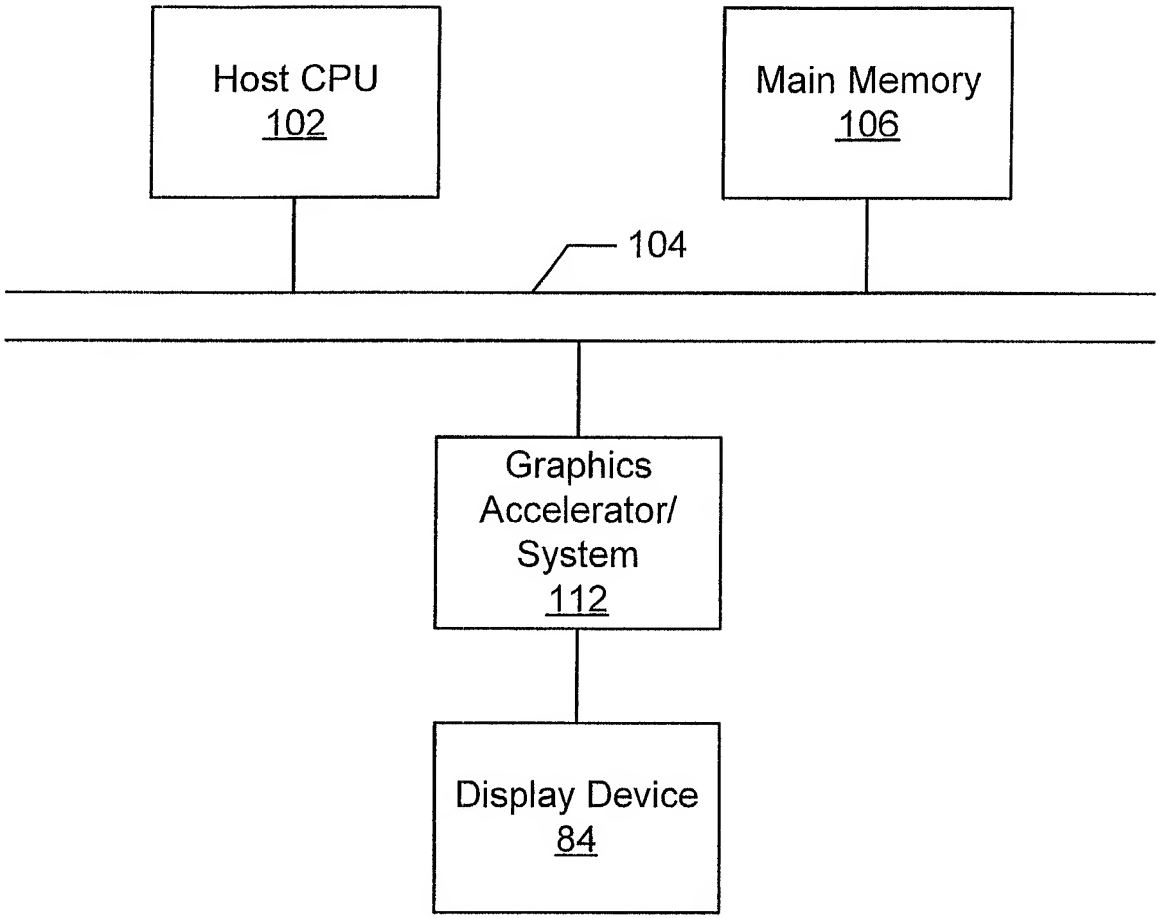

FIG. 2

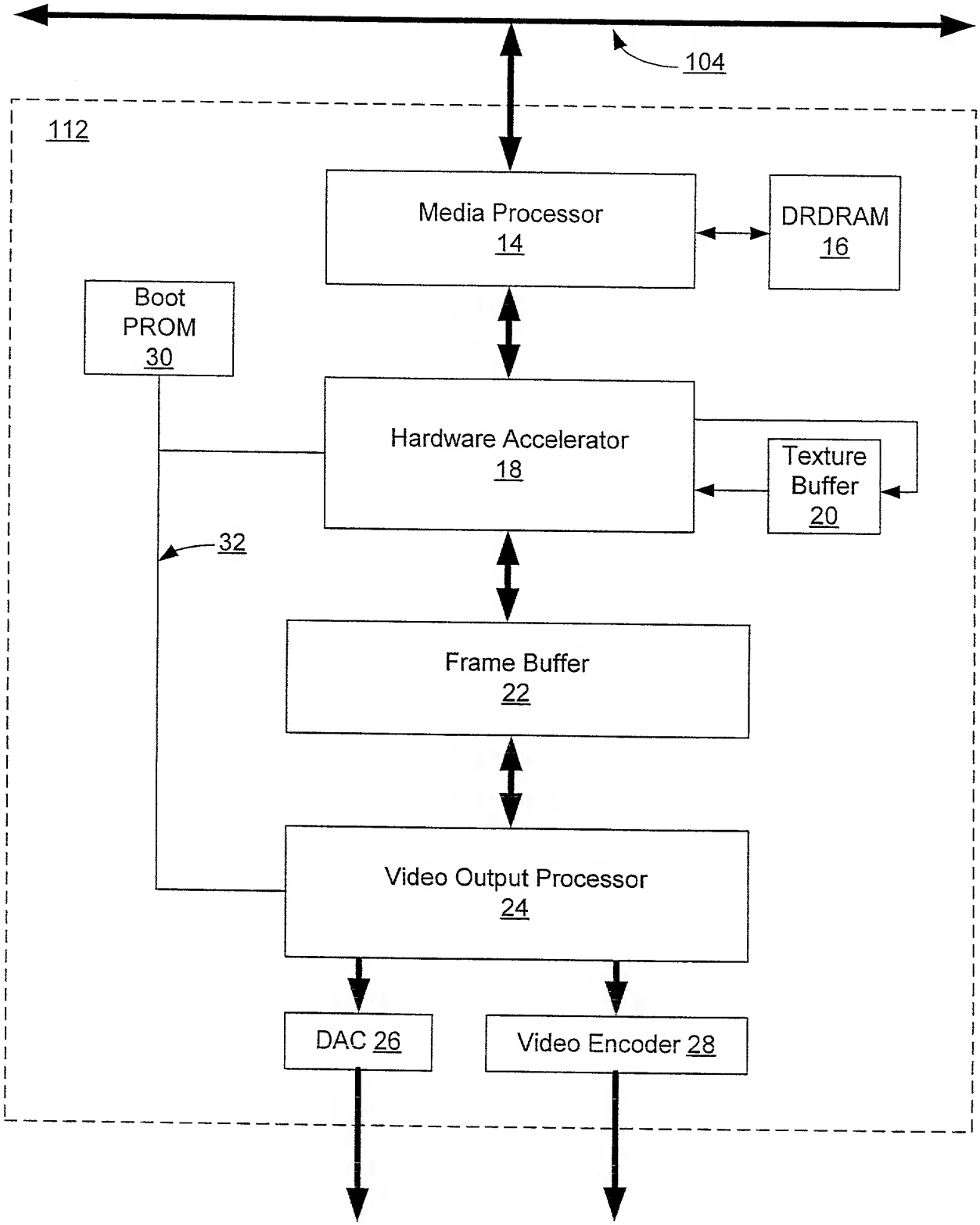
104
112
Media Processor
14
DRDRAM
16
Boot
PROM
30
Hardware Accelerator
18
Texture
Buffer
20
32
Frame Buffer
22
Video Output Processor
24
DAC 26
Video Encoder 28

FIG. 3

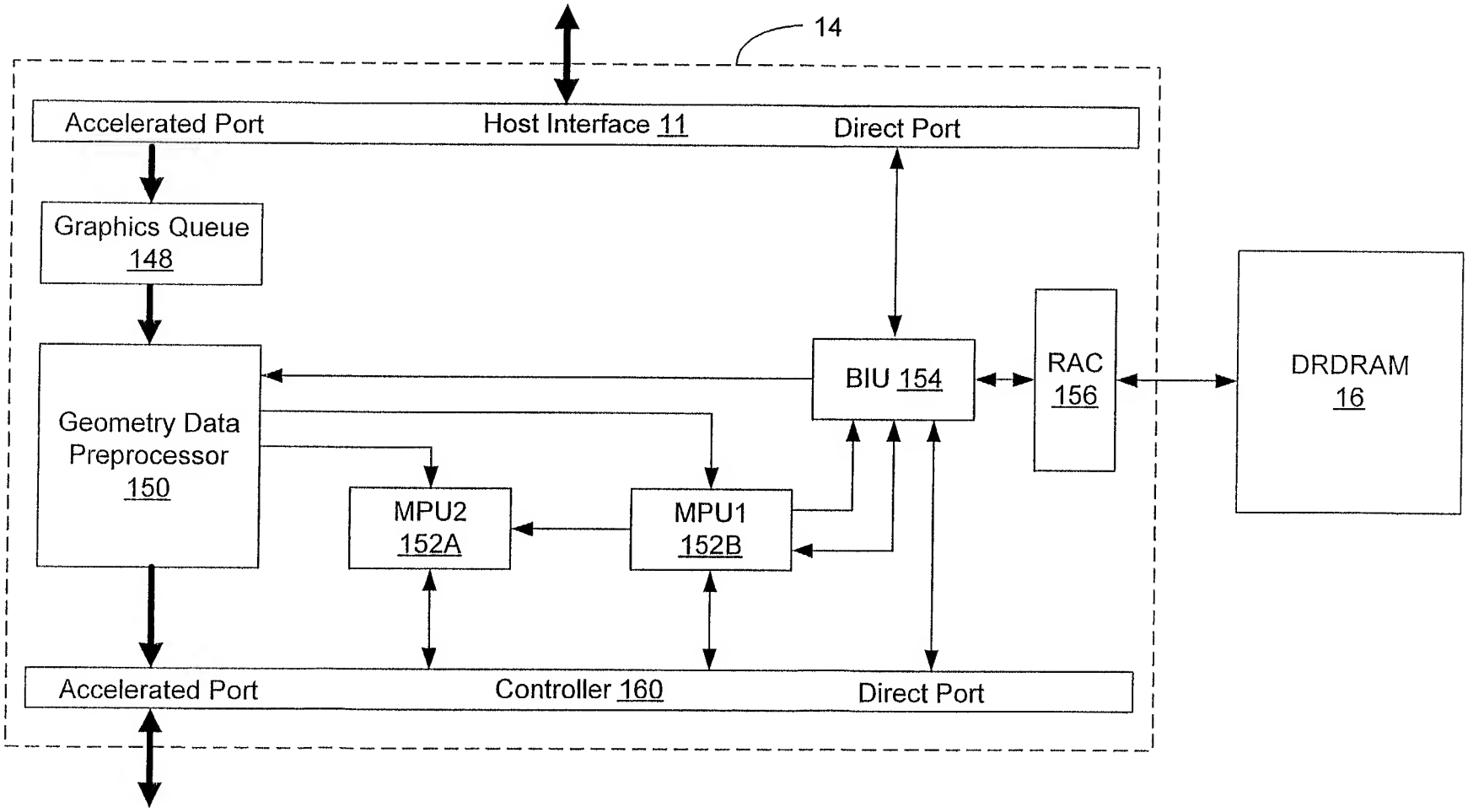
14
Accelerated Port
Host Interface 11
Direct Port
Graphics Queue
148
Geometry Data
Preprocessor
150
BIU 154
RAC
156
DRDRAM
16
MPU2
152A
MPU1
152B
Accelerated Port
Controller 160
Direct Port

FIG. 4

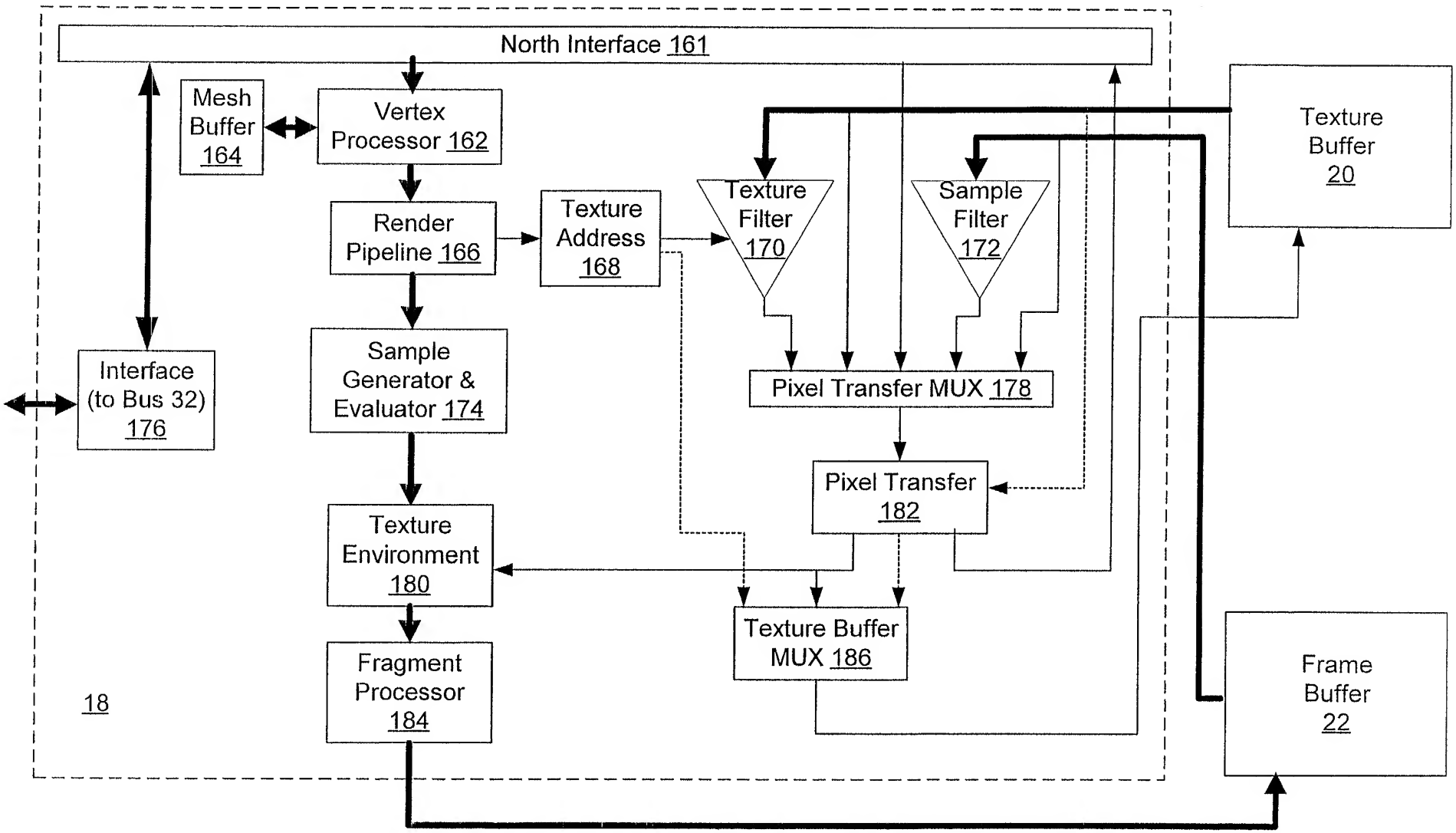
North Interface 161
Mesh Buffer 164
Vertex Processor 162
Render Pipeline 166
Texture Address 168
Texture Filter 170
Sample Filter 172
Texture Buffer 20
Interface (to Bus 32) 176
Sample Generator & Evaluator 174
Pixel Transfer MUX 178
Pixel Transfer 182
Texture Environment 180
Texture Buffer MUX 186
Fragment Processor 184
Frame Buffer 22
18

FIG. 5

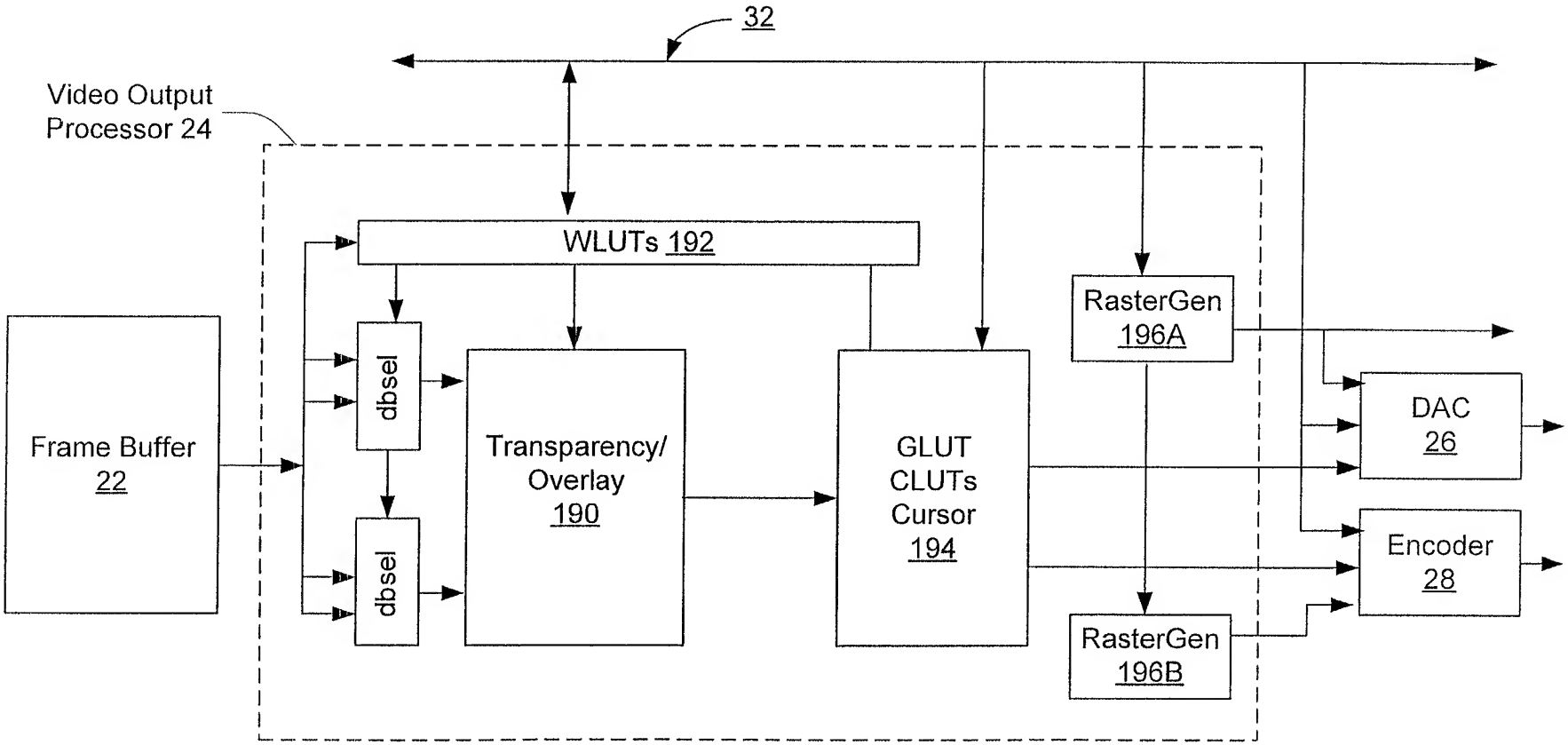
32
Video Output
Processor 24
WLUTs 192
Frame Buffer
22
dbsel
dbsel
Transparency/
Overlay
190
GLUT
CLUTs
Cursor
194
RasterGen
196A
RasterGen
196B
DAC
26
Encoder
28

FIG. 6

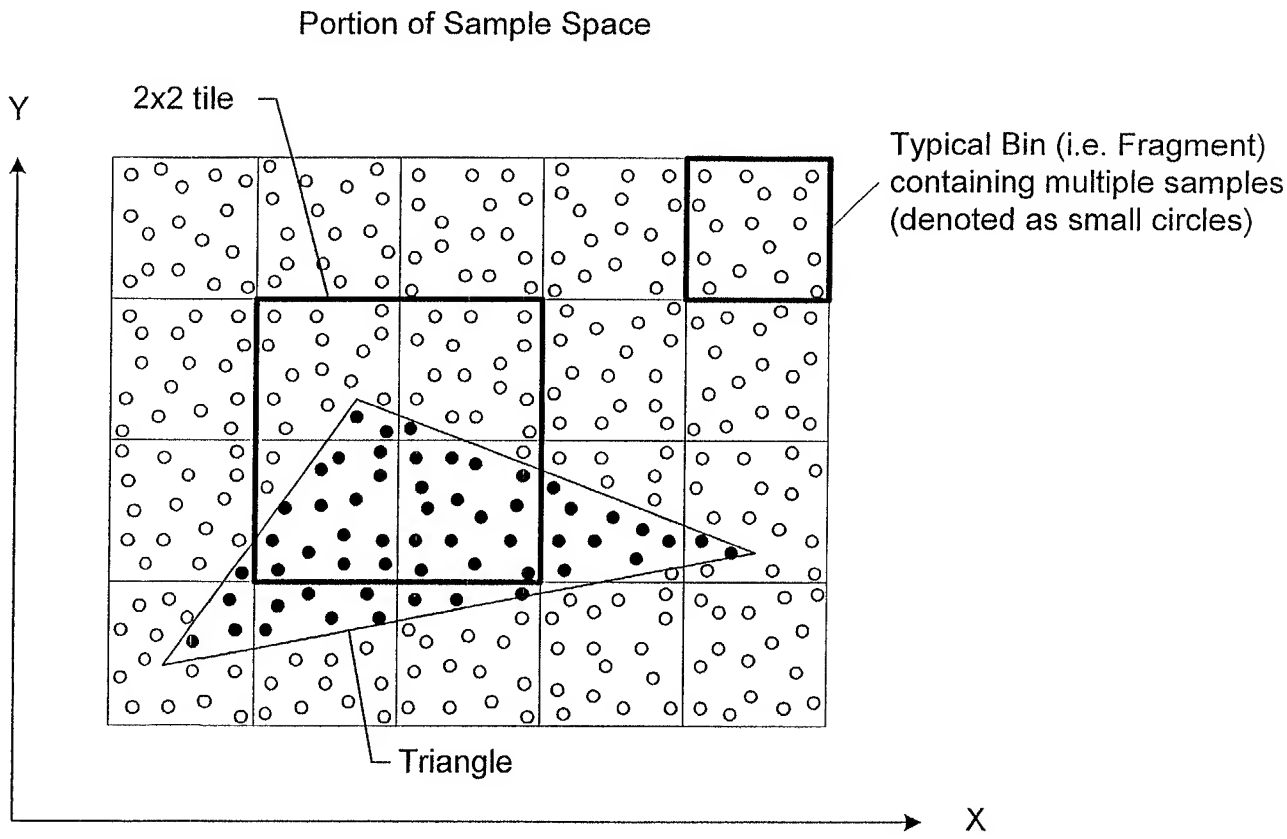
Portion of Sample Space
Y
2x2 tile
Typical Bin (i.e. Fragment)
containing multiple samples
(denoted as small circles)
Triangle
X

Fig. 7

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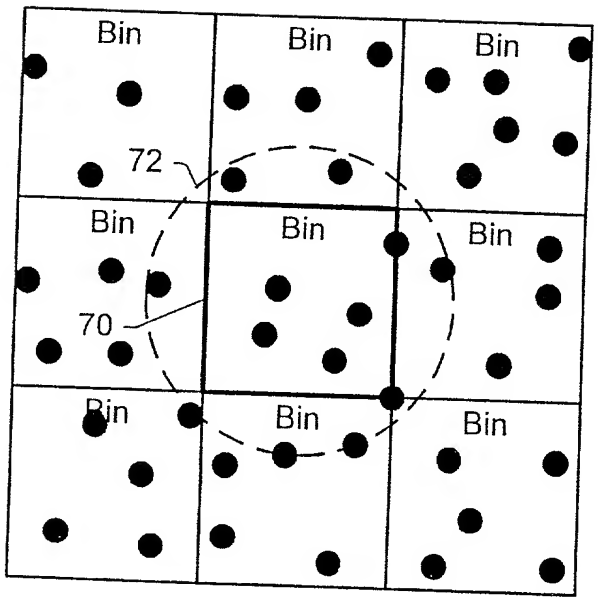


Fig. 8

208220 9E9580DT

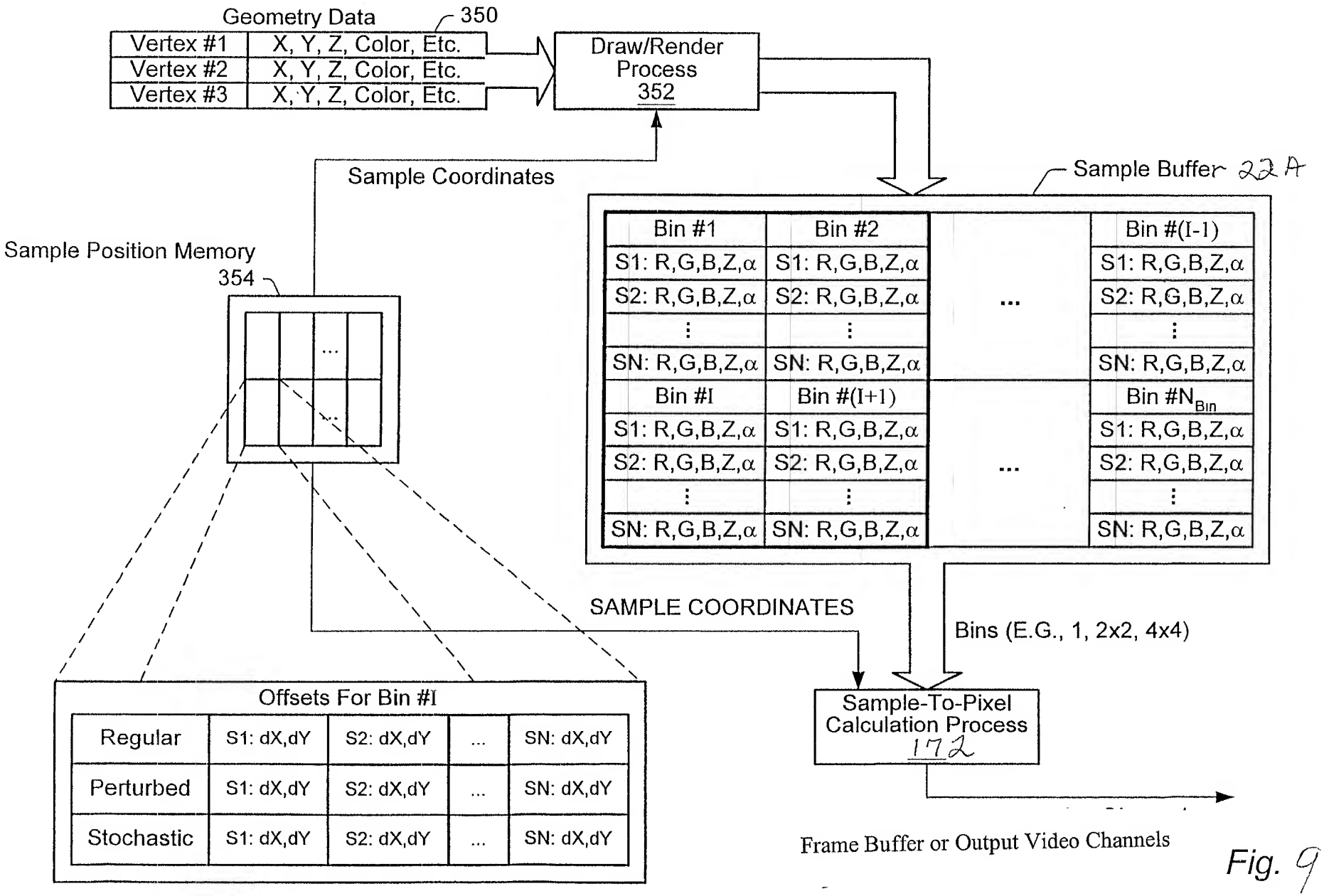


Fig. 9

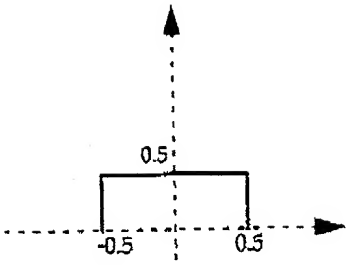


Figure 10A

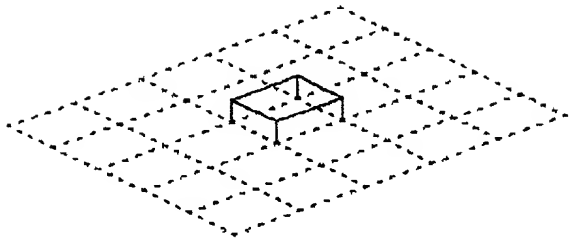


Figure 10B

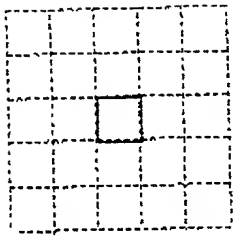


Figure 10C

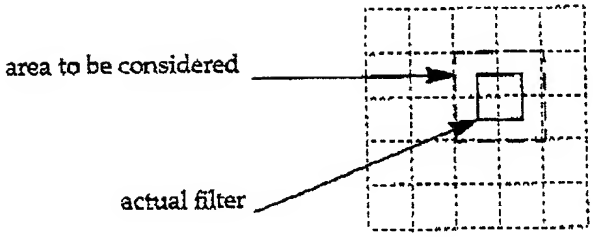
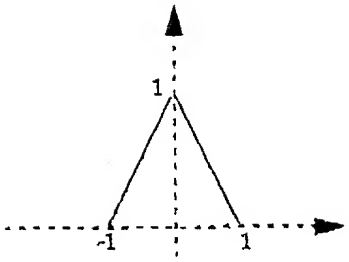
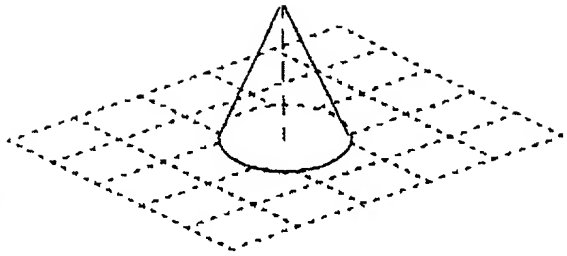


Figure 10D

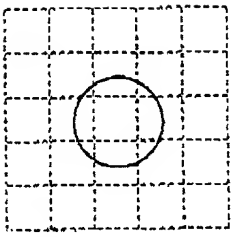
Patent - 6,252,608



11A



11B



11C

5,959,638 - 05/28/99

20020 "9E9S800T

1008526 - 052805

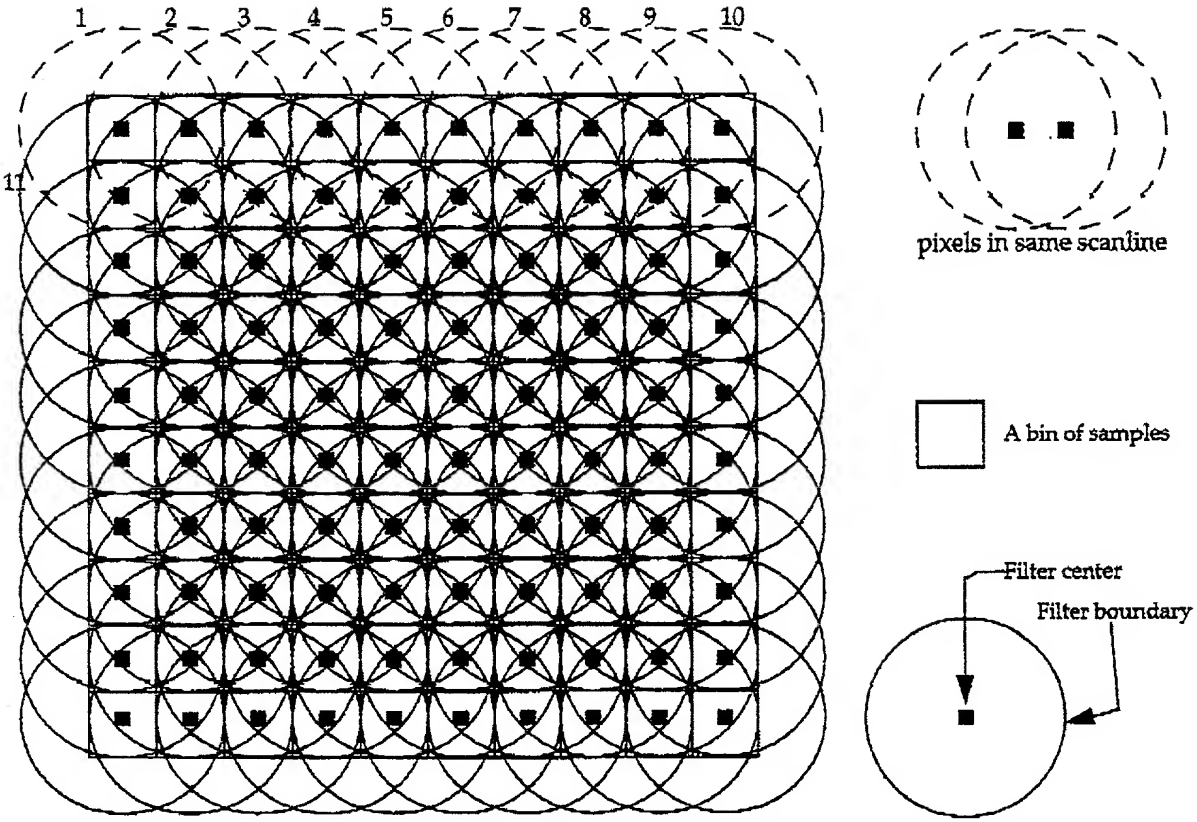
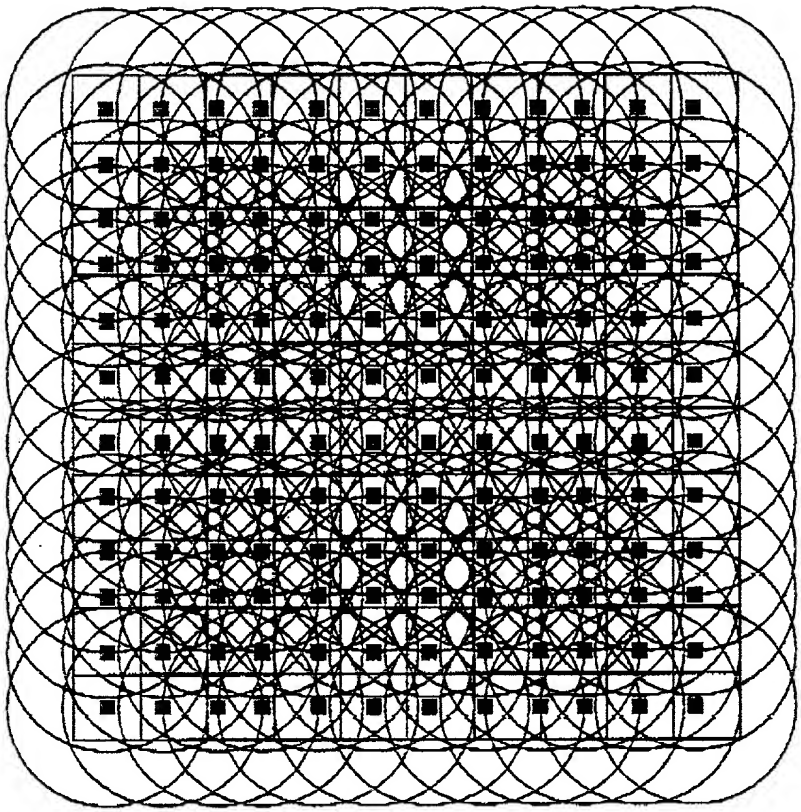


Figure 14

Application Copy



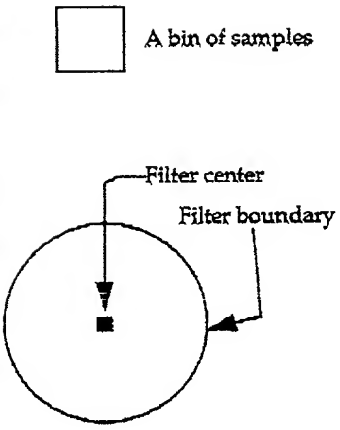
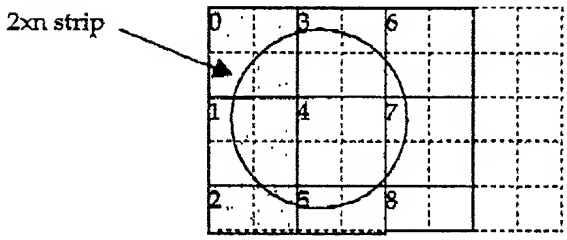
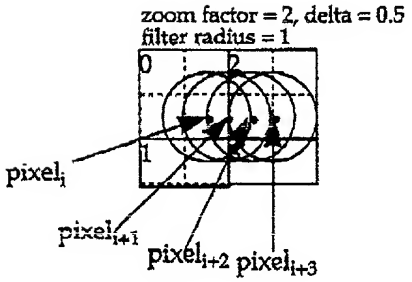


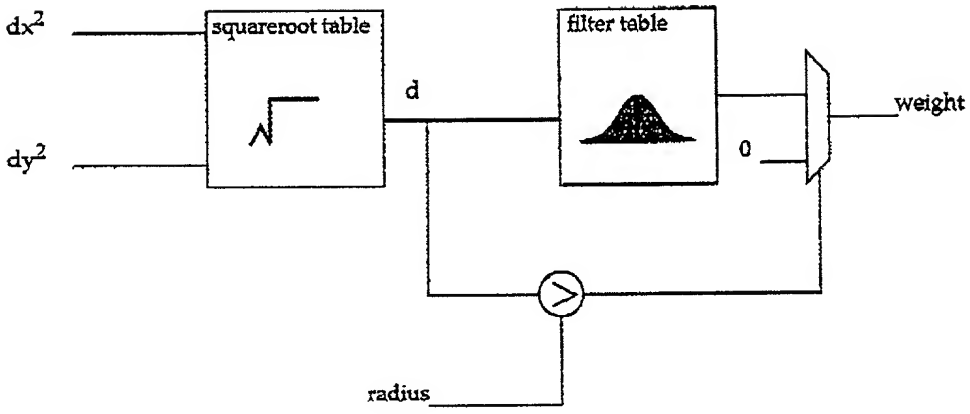
Fig. 5

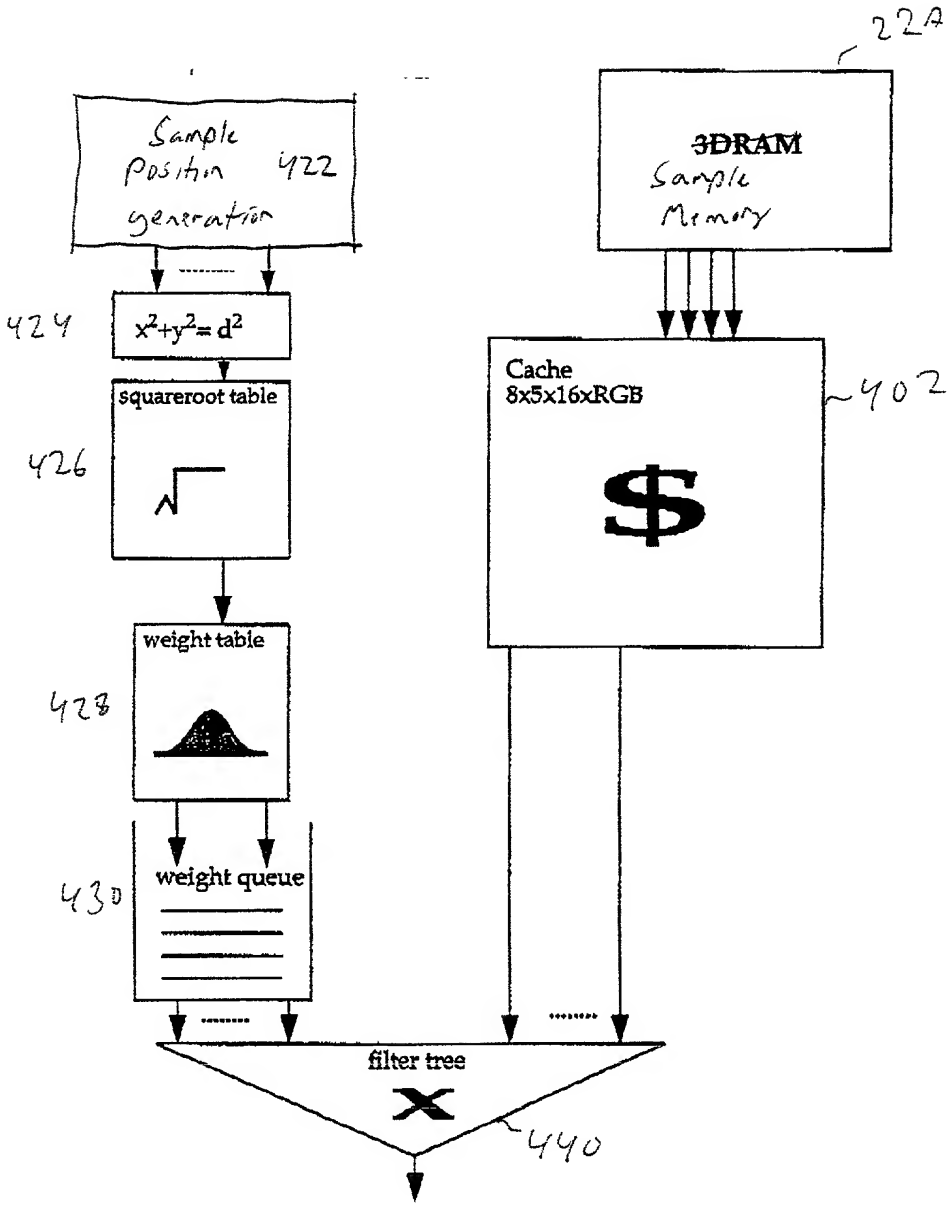

2xn strip
0
3
6
1
4
7
2
5
8

16

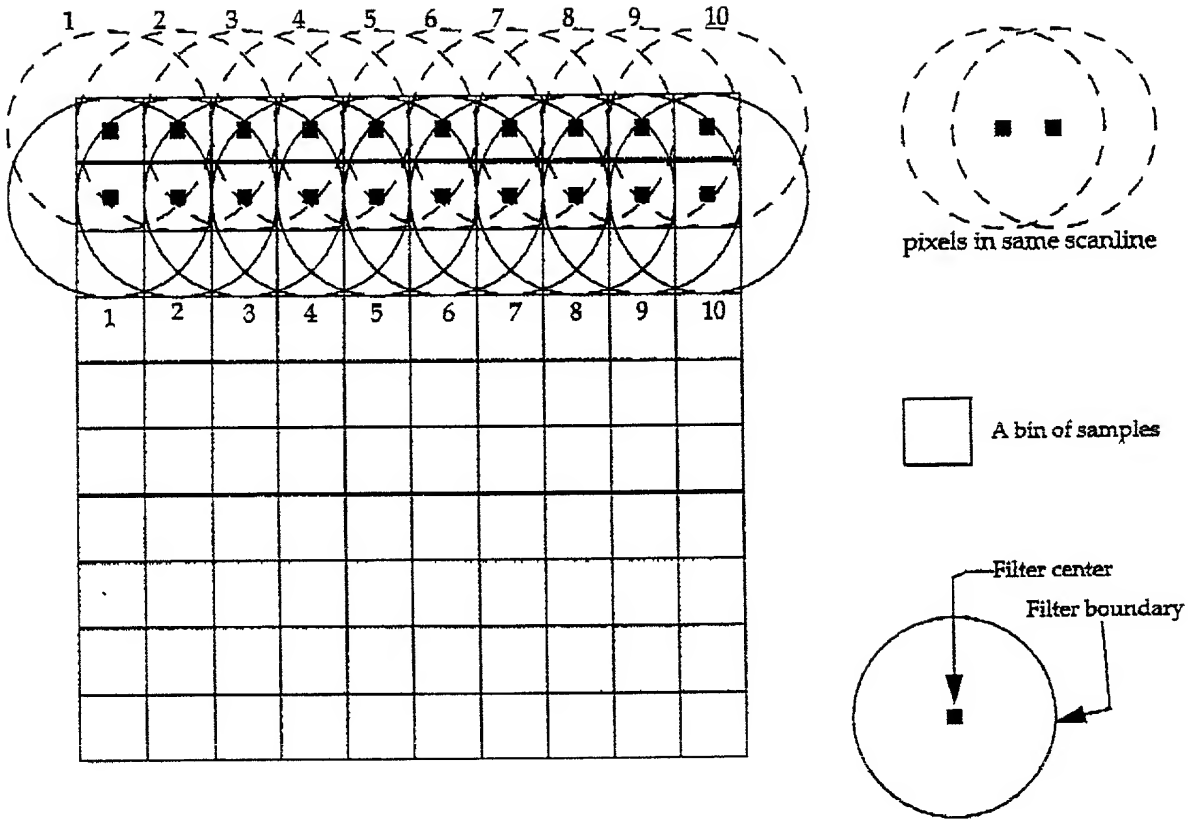

zoom factor = 2, delta = 0.5
filter radius = 1
0
2
1
pixel$_i$
pixel$_{i+1}$
pixel$_{i+2}$
pixel$_{i+3}$

17

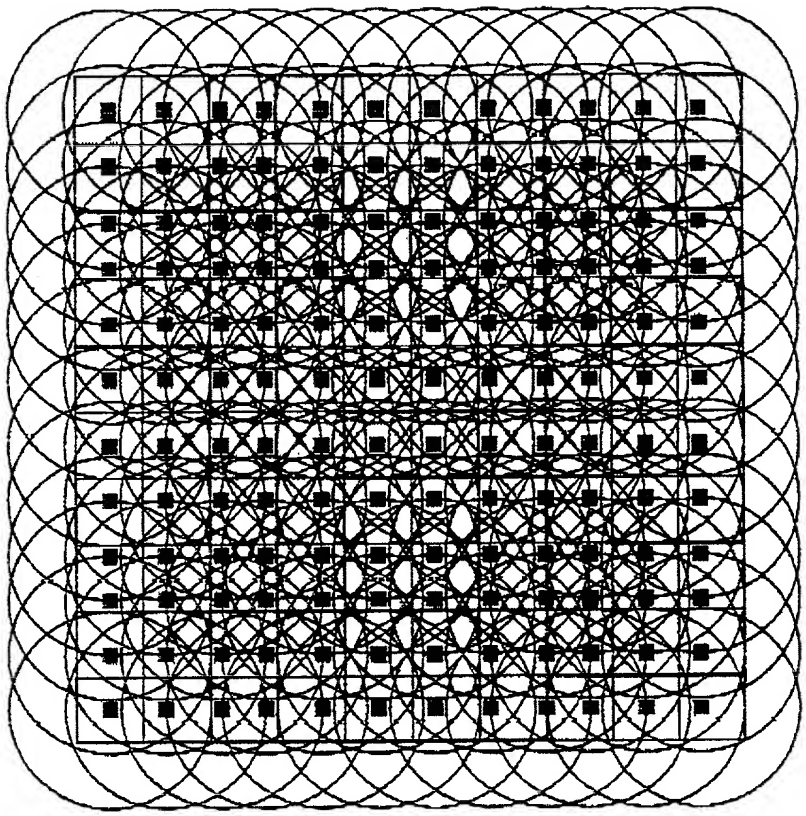

dx2
dy2
squareroot table
d
filter table
weight
0
radius

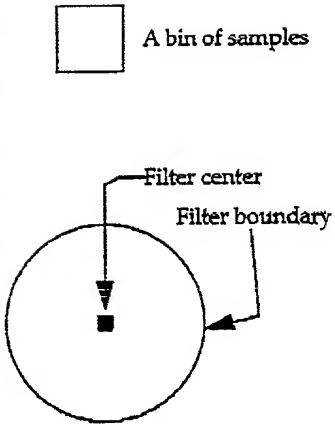

22A
Sample Position generation 422
3DRAM Sample Memory
424
$x^2+y^2=d^2$
squareroot table
426
Cache 8x5x16xRGB
402
weight table
428
weight queue
430
filter tree
440

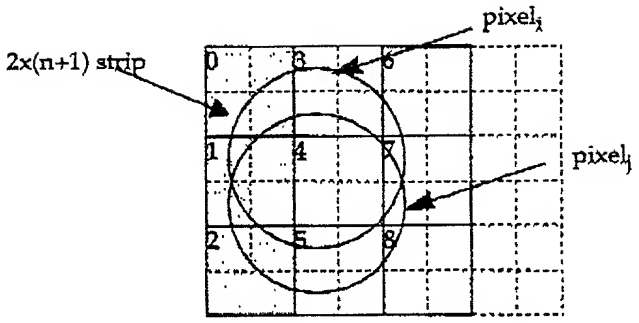
Adobe Systems



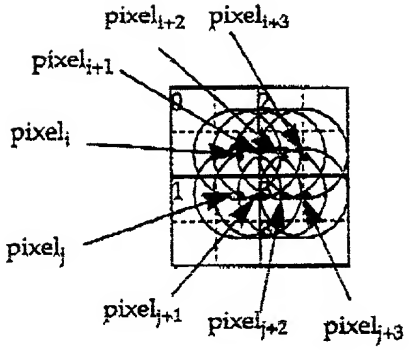
Document 95-95-0001







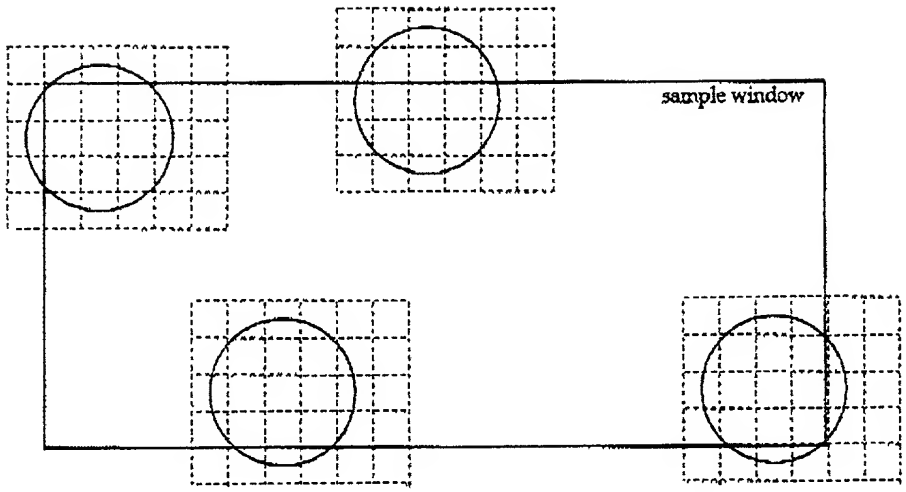
22



zoom factor = 2, delta = 0.5
filter radius = 1

23

HOBBS39 - 8/29/98



24

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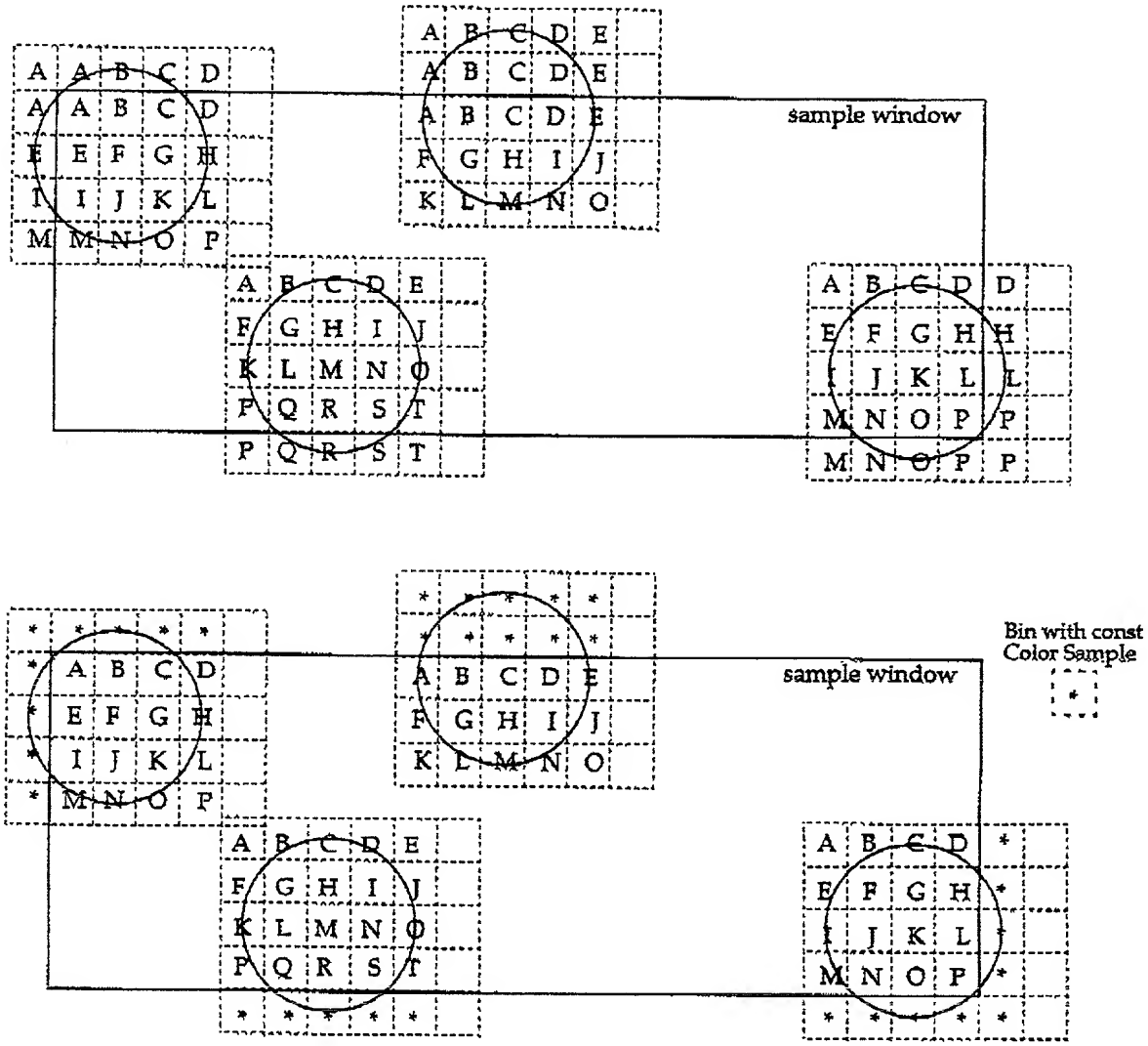
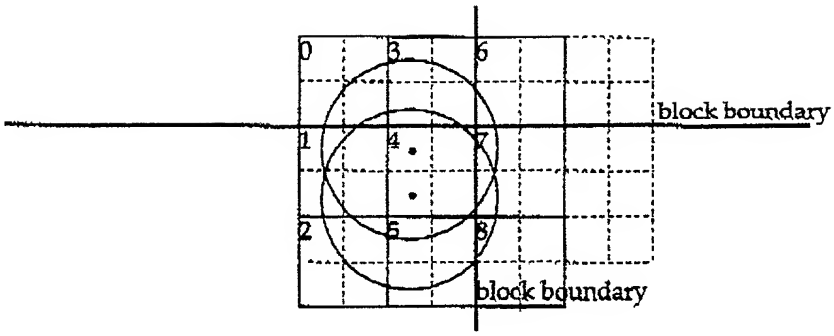
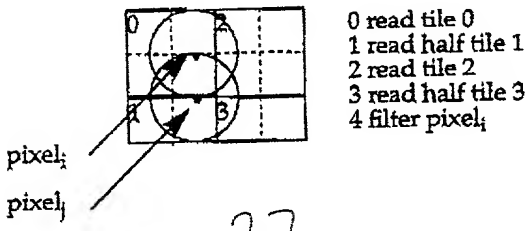


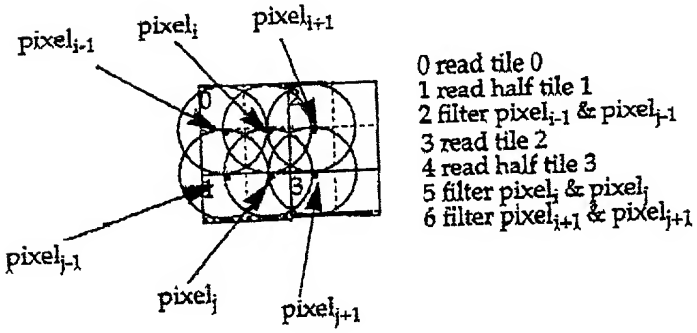
Figure 25



26

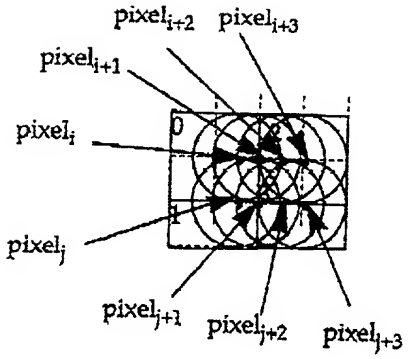


27



28

Exhibit 2009



0 read tile 0
1 read half tile 1
2 read tile 2
3 read half tile 3
4 filter pixel$_i$& pixel$_j$
5 filter pixel$_{i+1}$& pixel$_{j+1}$
6 filter pixel$_{i+2}$& pixel$_{j+2}$
7 filter pixel$_{i+3}$& pixel$_{j+3}$

29

For Non-Buddy Mode:

binInlv [1:0] \ sample[1:0]	0	1	2	3
0	a	b	c	d
1	c	d	a	b
2	d	c	b	a
3	b	a	d	c

where a, b, c, d identify different interleave bus to 3DRAM

For Buddy Mode:

binInlv [1:0] \ sample[2:0]	0	1	2	3	4	5	6	7
0	a	a	b	b	c	c	d	d
1	c	c	d	d	a	a	b	b
2	d	d	c	c	b	b	a	a
3	b	b	a	a	d	d	c	c

where a, b, c, d identify different interleave bus to 3DRAM

— Figure 30

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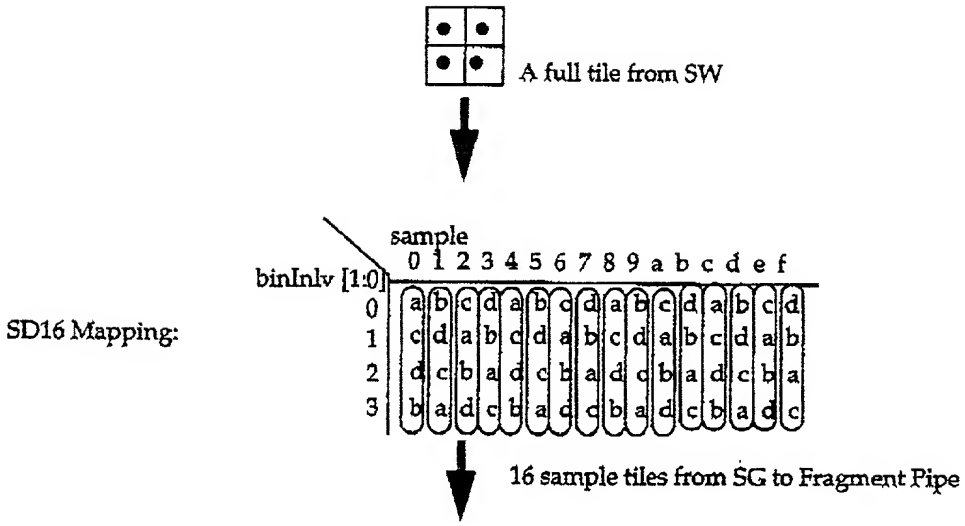
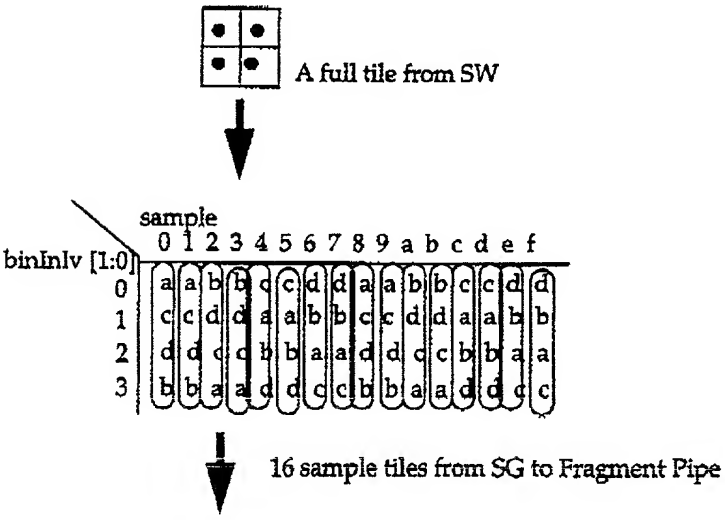
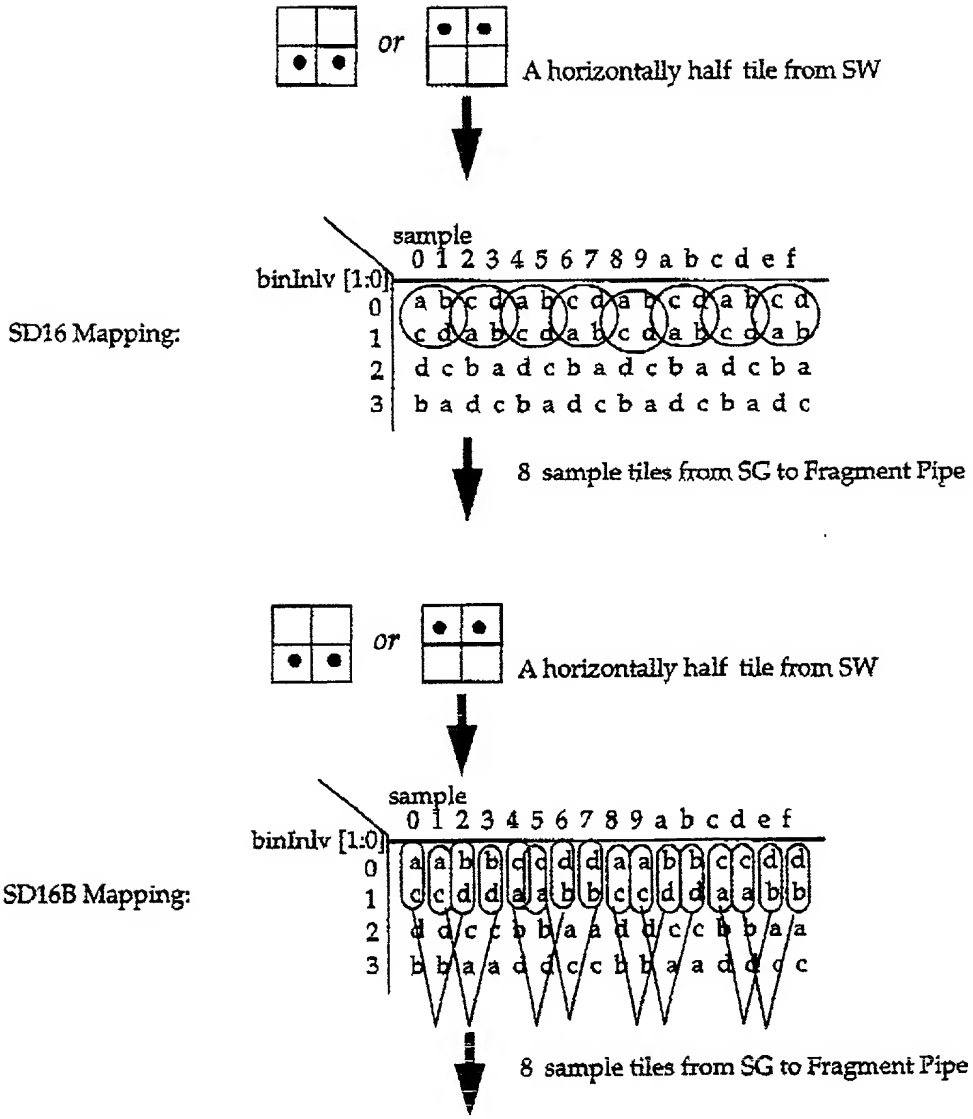


SD16 Mapping:



SD16B Mapping:



SD16 Mapping:

SD16B Mapping:

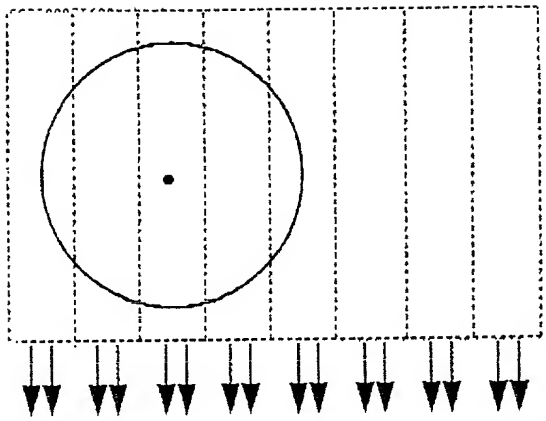


Fig 33

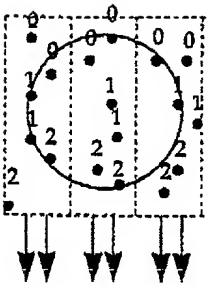
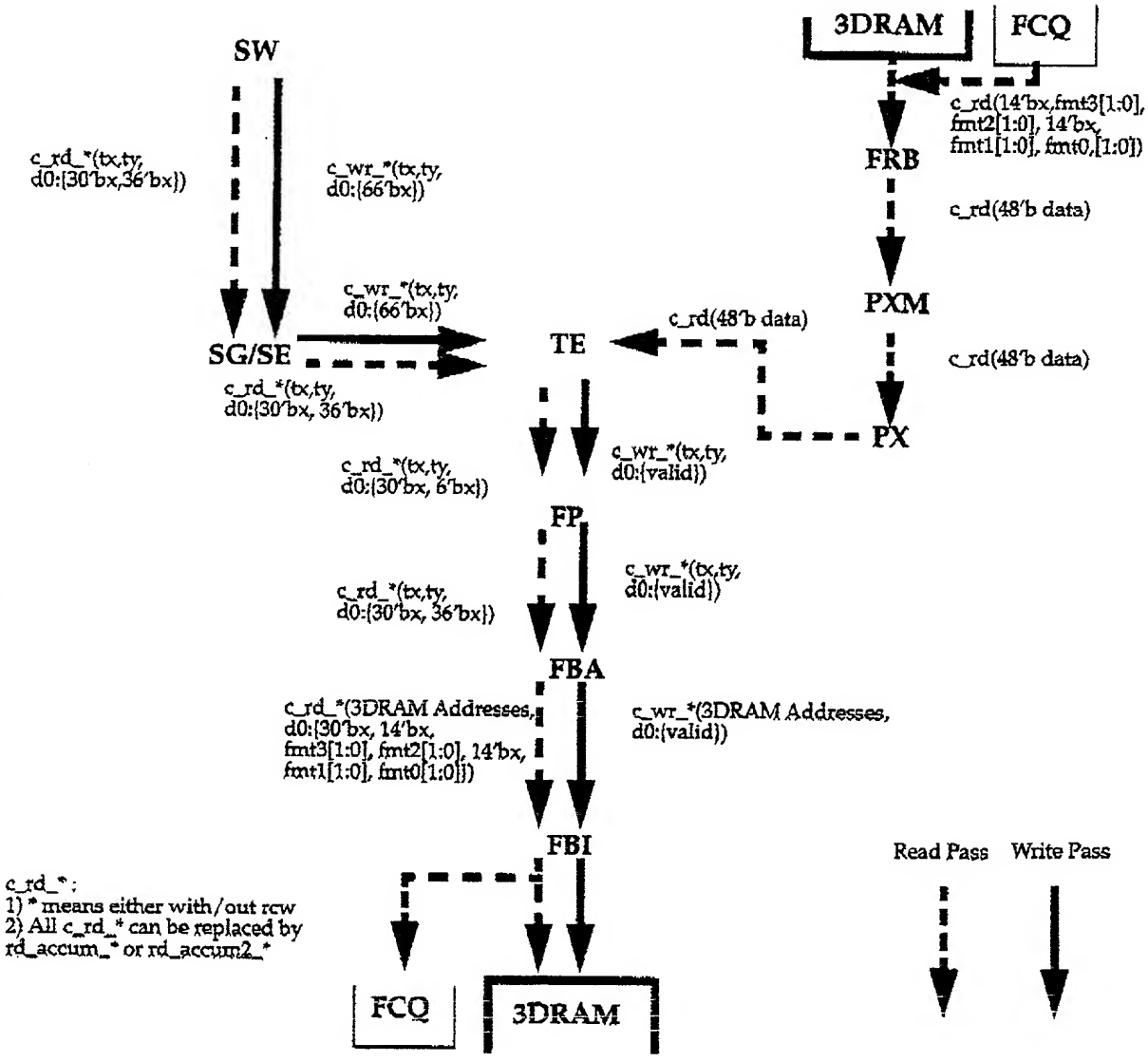


Fig 34

US005595902A



HDS5536 - 0025602

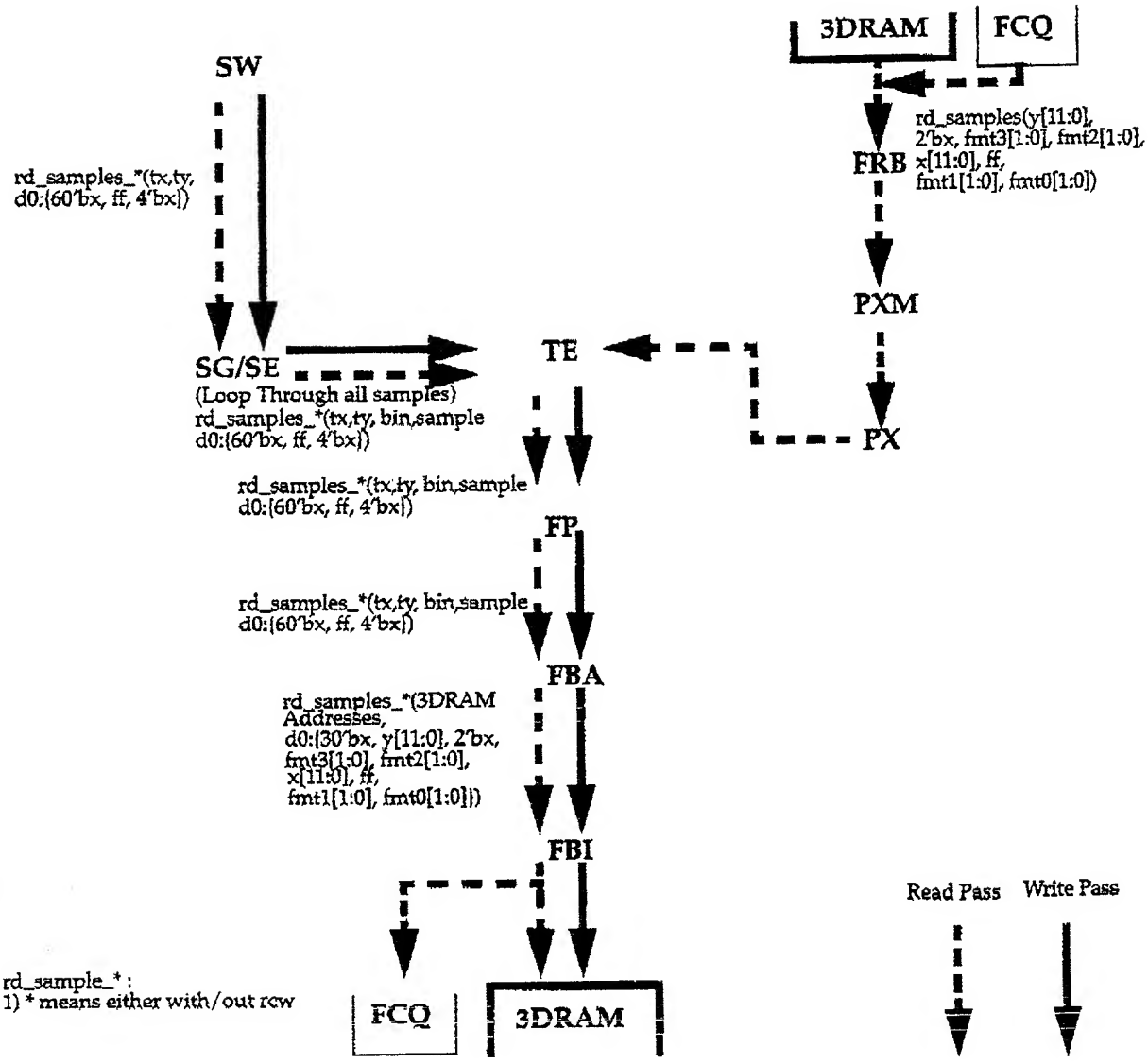

3DRAM
FCQ
SW
rd_samples(y[11:0], 2'bx, fmt3[1:0], fmt2[1:0], x[11:0], ff, fmt1[1:0], fmt0[1:0])
FRB
rd_samples_*(tx,ty, d0:{60'bx, ff, 4'bx})
PXM
TE
SG/SE
(Loop Through all samples)
rd_samples_*(tx,ty, bin,sample d0:{60'bx, ff, 4'bx})
PX
rd_samples_*(tx,ty, bin,sample d0:{60'bx, ff, 4'bx})
FP
rd_samples_*(tx,ty, bin,sample d0:{60'bx, ff, 4'bx})
FBA
rd_samples_*(3DRAM Addresses, d0:{30'bx, y[11:0], 2'bx, fmt3[1:0], fmt2[1:0], x[11:0], ff, fmt1[1:0], fmt0[1:0]})
FBI
Read Pass
Write Pass
rd_sample_* :
1) * means either with/out rcw
FCQ
3DRAM

Fig 36

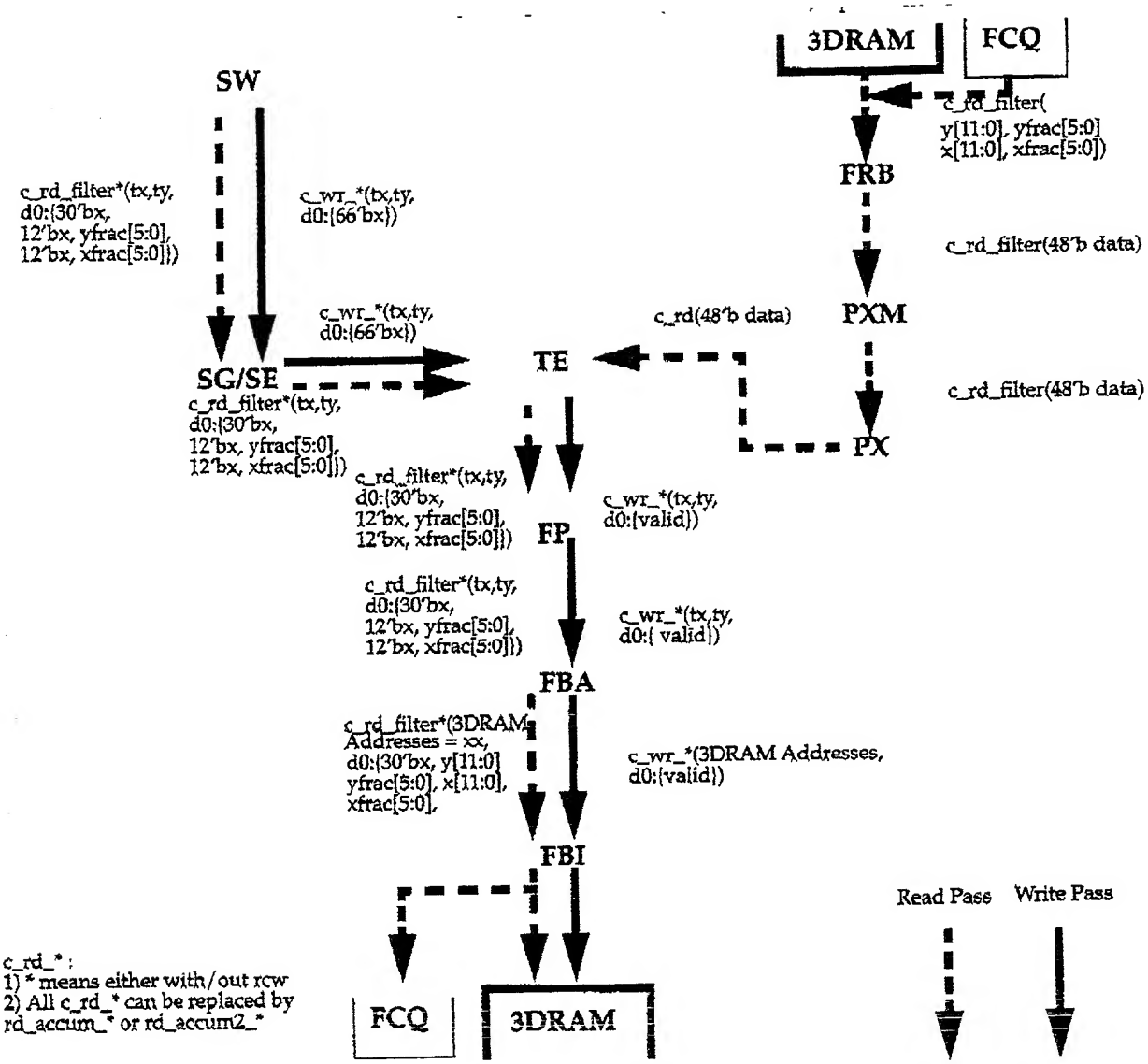

3DRAM
FCQ
SW
c_rd_filter(
y[11:0], yfrac[5:0]
x[11:0], xfrac[5:0])
FRB
c_rd_filter*(tx,ty,
d0:{30'bx,
12'bx, yfrac[5:0],
12'bx, xfrac[5:0]})
c_wr_*(tx,ty,
d0:{66'bx})
c_rd_filter(48'b data)
c_wr_*(tx,ty,
d0:{66'bx})
c_rd(48'b data)
PXM
TE
SG/SE
c_rd_filter*(tx,ty,
d0:{30'bx,
12'bx, yfrac[5:0],
12'bx, xfrac[5:0]})
c_rd_filter(48'b data)
PX
c_rd_filter*(tx,ty,
d0:{30'bx,
12'bx, yfrac[5:0],
12'bx, xfrac[5:0]})
c_wr_*(tx,ty,
d0:{valid})
FP
c_rd_filter*(tx,ty,
d0:{30'bx,
12'bx, yfrac[5:0],
12'bx, xfrac[5:0]})
c_wr_*(tx,ty,
d0:{ valid})
FBA
c_rd_filter*(3DRAM
Addresses = xx,
d0:{30'bx, y[11:0]
yfrac[5:0], x[11:0],
xfrac[5:0],
c_wr_*(3DRAM Addresses,
d0:{valid})
FBI
Read Pass
Write Pass
c_rd_* :
1) * means either with/out rcw
2) All c_rd_* can be replaced by
rd_accum_* or rd_accum2_*
FCQ
3DRAM

Fig 37